Program : **Diploma in Electronics and Communication Engineering / Electronics Engineering**	
Course Code : **5209**	Course Title: **Verilog HDL and PLD Lab**
Semester :**5 / 6**	Credits: **1.5**
Course Category: **Program Core / Elective**	
Periods per week: **3 (L:0, T:0, P:3)**	Periods per semester: **45**

Course Objectives:

1. To introduce the simulation and test functional aspects of digital electronics circuits using Gate level, Data flow, Behavioural modelling of Verilog Hardware description language

2. To familiarize FPGA trainer kit

Course Prerequisites:

Topic	Course Code	Course Title	Semester
Working of electronic components like diode, transistors etc	2041	Basic Electronics	2
Basics of Electronic circuits	3043	Electronics Circuits	3
Logic gates, Combinational and sequential logic circuits	3044	Digital Electronics	3
Basic Concepts of programming	3045	Fundamentals of C Programming	3

Course Outcomes:

On completion of the course, the student will be able to :

CO	Description	Duration (Hours)	Cognitive level
CO1	Develop Verilog HDL program for designing combinational logic circuits using gate level modelling.	9	Applying
CO2	Develop Verilog HDL program for designing combinational and sequential logic circuits using data flow modelling.	9	Applying
CO3	Utilize behavioural modelling to design Sequential and Combinational logic circuits	9	Applying

CO4	Make use of FPGA / CPLD trainer kits to realize different combinational and sequential logic circuits	12	Applying
	Lab Exam	6	

CO - PO Mapping:

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7
CO1	3			3			
CO2	3			3			
CO3	3			3			
CO4	3			3			

3-Strongly mapped, 2-Moderately mapped, 1-Weakly mapped

Course Outline:

Module Outcomes	Description	Duration (Hours)	Cognitive Level
CO1	**Develop Verilog HDL program for designing combinational logic circuits using gate level modelling.**		
M1.01	Simulate and verify Verilog description of different logic gates	1.5	Applying
M1.02	Simulate and verify Verilog description of Boolean expressions	1.5	Applying
M1.03	Simulate and verify Verilog description for 1 bit full adder	1.5	Applying
M1.04	Simulate and verify Verilog description for 4:1multiplexer	1.5	Applying
M1.05	Simulate and verify Verilog description for 1:4demultiplexer	1.5	Applying
M1.06	Simulate and verify Verilog description for 2-4 decoder	1.5	Applying
CO2	**Develop Verilog HDL program for designing combinational and sequential logic circuits using data flow modelling**		
M2.01	Simulate and verify Verilog description for half adder using data flow operators.	1.5	Applying
M2.02	Simulate and verify Verilog description for 1-bit full adder using data flow modelling	1.5	Applying
M2.03	Simulate and verify Verilog description for 4:1 multiplexer using conditional operator	1.5	Applying

M2.04	Simulate and verify Verilog description for 1:4 demultiplexer using logic equation	1.5	Applying
M2.05	Simulate and verify Verilog description for D Flip Flop using data flow modelling	1.5	Applying
M2.06	Simulate and verify Verilog description for T Flip Flop using data flow modelling	1.5	Applying
	Lab Exam 1	3	
CO3	**Utilize behavioural modelling to design Sequential and Combinational logic circuits**		
M3.01	Simulate and verify Verilog description for half subtractor and full subtractor using behavioural modelling	3	Applying
M3.02	Simulate and verify Verilog description for 4:1 multiplexer using behavioural modelling	1.5	Applying
M3.03	Simulate and verify Verilog description for JK Flip Flop using behavioural modelling	1.5	Applying
M3.04	Simulate and verify Verilog description for 4 bitshift register using behavioural modelling	1.5	Applying
M3.05	Simulate and verify Verilog description for 4 bitripple up counter using behavioural modelling	1.5	Applying
CO4	**Make use of FPGA / CPLD trainer kits to realize different sequential and combinational circuits**		
M4.01	Implement a 4-bit parallel adder using trainer kit	3	Applying
M4.02	Implement binary to gray code converter using trainer kit	3	Applying
M4.03	Implement BCD to 7 segment decoder using trainer kit	3	Applying
M4.04	Implement a 4 bit Ripple up counter using a trainer kit	3	Applying
	Lab Exam 2	3	

Text / Reference Books

T/R	Book Title/ Author
T1	Verilog HDL –Samir Palnitkar-Pearson Education
T2	Digital design Morris mano, Third Edition, PHI

T3	FPGA protyping by Verilog examples –PONG P Chu - Willey
R1	FPGA based system design Wayne Wolf, Pearson Education
R2	T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
R3	HDL Programming- Nazeih M Botros- Dream Tech
R4	Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
R5	Digital Systems Design with FPGAs and CPLDs -Ian Grout, Elsevier

Online Recourses:

Sl.No	Website Link
1	https:/nptel.ac.in/courses/106/105/106105165/
2	https://www.tutorialspoint.com/vlsi_design/vlsi_design_verilog_introduction.htm
3	https://www.youtube.com/watch?v=PJGvZSlsLKs
4	https://www.youtube.com/watch?v=pR6-aNxHNac

Suggested open ended experiments

1. Develop Verilog HDL program for Traffic Signal Control for a junction where 4 roads meets.
2. Design an 8 function ALU that takes 4 bits inputs A and B and a 3-bit input select, and gives a 5-bit output out.
3. Develop a coffee vending machine using Verilog HDL programming.